WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

an element isolation part surrounding one element formation region when viewed in the direction perpendicular to a main surface of a semiconductor substrate and electrically isolating the one element formation region from another element formation regions; and

a plurality of elements provided in said element formation region, wherein

said plurality of elements includes a first field-effect transistor and a second field-effect transistor functioning as high side switches of a latch circuit,

said semiconductor device is utilized in the state where a lower side of one of said first field-effect transistor and said second field-effect transistor is completely depleted, and

said first field-effect transistor and said second field-effect transistor share a source region or a drain region.

2. The semiconductor device according to claim 1, wherein

said first field-effect transistor and said second field-effect transistor are P-channel field-effect transistors, respectively.

3. The semiconductor device according to claim 1, wherein

said first field-effect transistor is a P-channel field-effect transistor, and

said second field-effect transistor is a P-channel insulated gate bipolar transistor.

4. The semiconductor device according to claim 1, wherein

said first field-effect transistor is a P-channel field-effect transistor, and

said second field-effect transistor is an N-channel field-effect transistor.

5. The semiconductor device according to claim 1, wherein said semiconductor device comprises:

the semiconductor substrate of a first conductive type;

an impurity diffusion layer of a second conductive type, formed on the semiconductor substrate of the first conductive type so as to cover the semiconductor substrate of the first conductive type, on which said first field-effect transistor and said second field-effect transistor are provided;

an impurity diffusion region of the first conductive type formed inside the impurity diffusion layer of the second conductive type and connected to a source electrode or a drain electrode of one of said first field-effect transistor and said second field-effect transistor; and

an impurity diffusion region of the second conductive type, having an impurity concentration higher than that of said impurity diffusion layer of the second conductive type, located between the impurity diffusion region of the first conductive type and said semiconductor substrate of the first conductive type.

6. A semiconductor device comprising: a first field-effect transistor having a channel region of a first conductive type; and a second field-effect transistor having a channel region of a second conductive type which is a conductive type opposite to said first conductive type,

the gate electrode of said first field-effect transistor and the drain electrode of said second field-effect transistor being integrally formed of the same conductive layer and extending in sequence in a predetermined direction in a linear manner, and

the source electrode of said first field-effect transistor and the source electrode of said second field-effect transistor being integrally formed of the same conductive layer and extending in sequence in a predetermined direction in a linear manner, wherein

the difference in potential between the source electrode of said first field-effect transistor and the drain electrode of said second field-effect transistor is approximately the same as the difference in potential between the gate electrode and the source electrode of said first field-effect

transistor, and

the punch through voltage between the impurity diffusion region of the second conductive type beneath the drain electrode of said second field-effect transistor and the impurity diffusion region of the second conductive type beneath the gate electrode of said first field-effect transistor is greater than the difference in potential between the source electrode of said first field-effect transistor and the drain electrode of said second field-effect transistor.